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Study for the Reliability of Nano-Scale MOS Devices that Experienced Implantation of Hydrogen or Deuterium at the Back-End of the Process Line

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This paper is focused on the improvement of MOS device reliability related to hydrogen or deuterium atoms. The injection of these atoms into the gate oxide film was achieved through low-energy implantation at the back-end of a line for the purpose of passivation of dangling bonds at the SiO_2/Si interface. Experimental results are presented for the degradation of the 3-nm-thick gate oxide (SiO_2) under both hot-carrier-injection (HCI) and constant voltage stresses using p- and n-MOSFETs. Device parameters, as well as the gate leakage current, depend on the degradation of gate oxide and, compared to corresponding hydrogen incorporation, are improved by deuterium incorporation. The Si-D bonds (instead of Si-H) in the SiO_2 film were found to play a major role in suppressing the generation of oxide traps. However, when the concentration of deuterium is redundant in the gate oxide, excess traps are generated and degrade the performance. Our result suggests a novel method to incorporate deuterium in the MOS structure for reliability.

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Keywords: Gate oxide, MOS device, Reliability, Deuterium, Hydrogen, Implantation

I. INTRODUCTION

The reliability of thin gate oxides is one of the important issues for the miniaturization of nano-scale MOS devices. The electrical degradation of MOS transistors due to electrical stresses, such as channel hot carrier injection (HCI), the negative-bias temperature instability (NBTI), and the stress-induced leakage current (SILC), has been extensively studied [1–3]. Some degradations are related to the hydrogen release from the Si/SiO_2 (channel/gate-oxide) interface [4,5].

The process of post-metallization anneal of the wafers at a low temperatures in a hydrogen ambient is critical to Complementary MOS (CMOS) fabrication technology to improve device function by passivating the otherwise electrically active interface traps, but it sets the stage for subsequent hydrogen-related degradation. Hydrogen desorption from silicon dangling bonds is usually considered to be the dominant mechanism by which defects are created.

Recently, an alternative process during which the interface traps are passivated by deuterium instead of hydrogen has been demonstrated [6,7]. This phenomenon can be understood as a kinetic isotope effect. The chemical reaction rates involving the heavier isotopes are reduced; consequently, under electrical stress, bonds to deuterium are more difficult to break than bonds to hydrogen. Therefore, treatment with deuterium instead of hydrogen in CMOS fabrication provides a possible solution for the reliability issues.

However, it is difficult to identify whether the deuterium could passivate all the silicon dangling bonds along the gate length because a silicon-nitride layer over the transistor usually suppresses the diffusion of deuterium [8]. The question, whether a multilevel metallization or a SiN cap process renders the deuterium anneal ineffective, is a topic of current research.

In our study, hydrogen or deuterium atoms are incorporated near the gate oxide layer through low-energy implantation for the purpose of passivating the dangling bonds at the SiO_2/Si interface and non-bridging atoms in bulk- SiO_2. The implantation was done after the first metallization step, not to disturb the standard manufacturing process. Electrical stresses were achieved for the prepared p-type and n-type MOSFETs. The dependences of the device parameters, as well as the gate leakage current, on the implantation conditions were inves-

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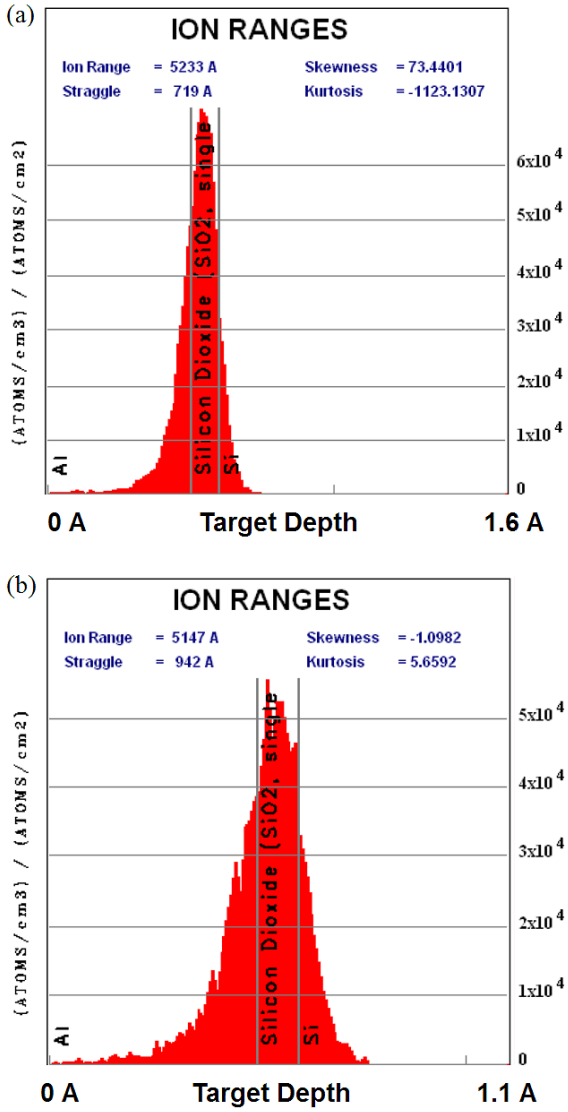

Fig. 1. Distribution of (a) hydrogen ions (60 keV) and (b) deuterium ions (45 keV) building up in the aluminum/SiO_2/silicon target. The distribution was simulated with the STIM tool. The ion range is about 5150 ∼ 5250 Å.

tigated. Finally, the result for our device was compared with that for conventionally annealed devices.

II. EXPERIMENTS

Both p- and n-MOSFETs were fabricated using standard CMOS processes for various channel lengths and widths down to 0.15 mm. The gate oxide thickness was 3 nm electrically. The gate oxide films were produced with a conventional furnace in a H_2-O_2 ambient. The implantation for the passivation was performed at the back end of the process line (after first metallization).

The transistors from a given wafer were divided into

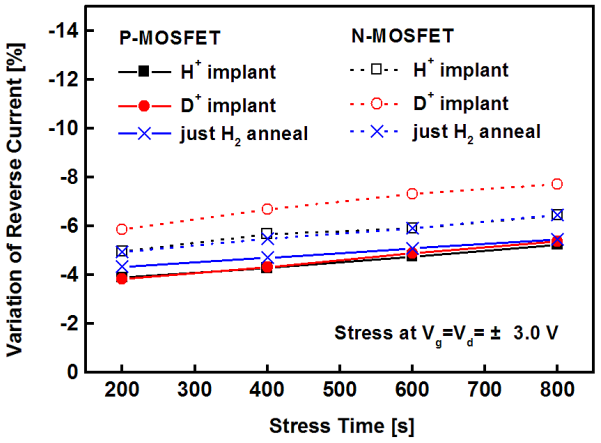

Fig. 2. Variation of reverse saturation drain current during HCI stress for hydrogen- or deuterium-implanted devices and for a conventionally annealed device. The conventional device was annealed in a H_2 ambient at 450 °C.

two groups. One group was implanted by H^+ ion at 60 keV, and the other group was implanted by D^+ ion at 45 keV. The ion dose was fixed at $1 \times 10^{14}/cm^2$ for the hydrogen implantation while in case of the deuterium implantation, the ion dose ranged from $1 \times 10^{14}/cm^2$ to $1 \times 10^{10}/cm^2$. Post-annealing was achieved at 400 °C for 30 minutes in a N_2 ambient for all the devices to activate the injected ions. The implantation conditions for each ion were extracted through the computer simulation (SRIM tool), as shown in Figure 1. The total thickness from the top of first metal to the bottom of the gate oxide was about 600 nm, including aluminum, silicon dioxide, and polysilicon layers. A control device was also prepared without our implantation process to compare its electrical properties with those of our processed devices.

A voltage of $V_g = V_d = \pm 3.0$ V was applied to the MOSFET gate at room temperature to accelerate the gate oxide degradation by HCI. The source terminal was connected to the substrate and the ground. For the gate-oxide leakage-current measurements, large area MOSFETs (W/L = 500 um/500 um) were used to avoid the edge effect, and a constant voltage, $V_g = \pm 3.5$ V, was applied to the gate terminal. The percent shifts (%) of the forward saturation drain current (I_F) and the reverse saturation drain current (I_R) were measured to determine the device parameter degradation. The percent shifts (%) of the gate current (I_g) were also monitored to assess the gate oxide wear-out.

III. RESULT

The performances of the transistors implanted with hydrogen or deuterium prior to electrical stress were not different in any region of operation. Figure 2 shows the

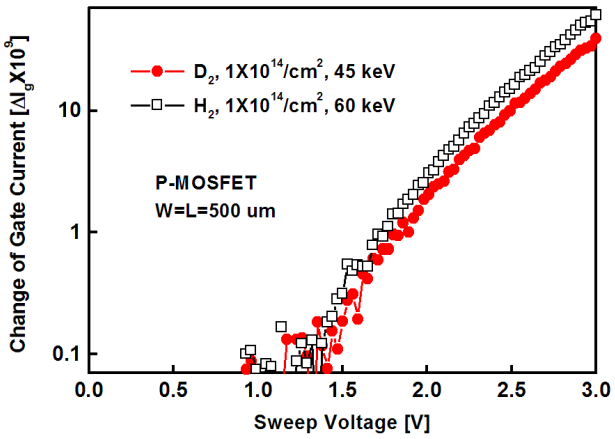

Fig. 3. Change of gate leakage current, after a constant voltage stress (V_g = 3.5 V), of large-area p-MOSFETs implanted with H_2 and D_2.

decrease in the reverse saturation current for p- and n-MOSFET measured after the HCI stress. The implantation dose was 1 × 10^{14}/cm^2 for both devices, but the implantation energy was different, 60 keV for H^+ and 45 keV for D^+, due to their different masses. The degradation for the processed transistors was compared with that for the conventional transistor. The degradation of the saturation current of the nano-scale MOSFET is usually related to the interface traps generated during the stress. In Figure 2, it appears that neither hydrogen nor deuterium implantation in this condition improves the reliability of transistor. The excess hydrogen or deuterium may accelerate the degradation of the gate oxide because interaction of electrical stress, and the hydrogen atom is somewhat the cause of the degradation. It is also difficult to find the isotope effect in the saturation current property between hydrogen- and deuterium-implanted transistors.

Contrary to the annealing process, the implant process can inject ions into the gate oxide with a certain uniformity. With conventional hydrogen annealing, hydrogen atoms usually pile up highly at the Si/SiO_2 interface. By using an optimum condition of implantation, one can implant atoms uniformly inside the gate oxide (oxide bulk). The variation of the gate oxide leakage current is used in the reliability to estimate the generation of oxide bulk traps inside the gate oxide [9].

Figure 3 presents the variation of gate current for both H^+- and D^+-implanted p-MOSFETs. The current was measured at the gate terminal while the gate voltage was being swept from 0 to 3 V. The device with deuterium implantation showed a lower gate leakage current for the entire range of sweeping voltages. Because the generation of stress-related bulk-oxide traps is suppressed by deuterium incorporation, we can infer that the isotope effect is valid in our new implant process. Therefore, deuterium implantation might be used to improve the reliability if a suitable implant condition is obtained.

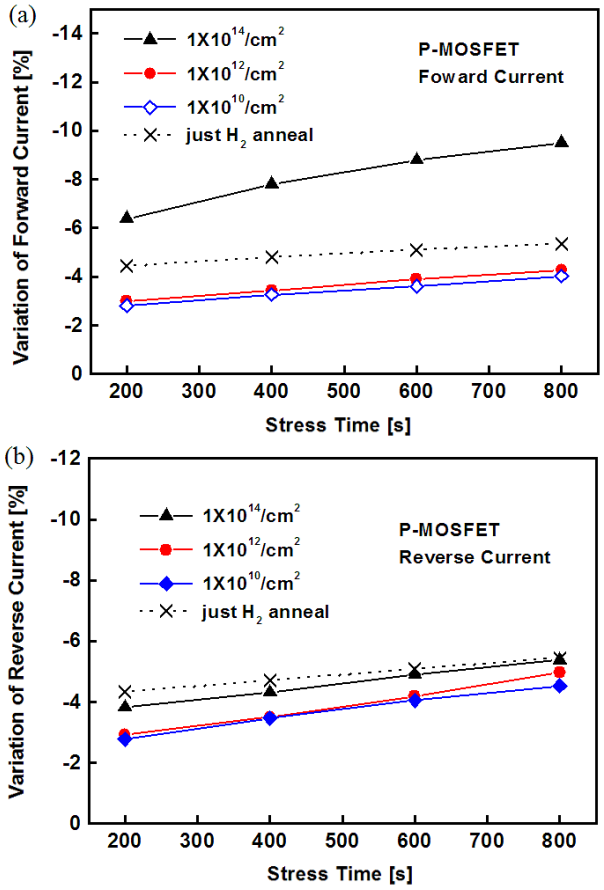

Fig. 4. Variations of the (a) forward, I_F, and the (b) reverse, I_R, saturation drain currents during HCI stress for deuterium-implanted p-MOSFETs. The implantation dose was changed from 1 × 10^{14}/cm^2 to 1 × 10^{10}/cm^2. The conventional device was annealed in a H_2 ambient at 450 °C.

Figures 4 and 5 present the influence of the deuterium dose on the degradation of performance for both p- and n-MOSFETs. The ion dose was changed from 1 × 10^{14}/cm^2 to 1 × 10^{10}/cm^2, and its effect was compared with that of the conventional H_2-annealed devices. The saturation drain current was measured at both forward and reverse modes. In the forward mode, the physical property of the gate oxide near the drain region is reflected in the electrical properties while in the reverse mode, that near the source region is reflected. From the figures, the dose of 1 × 10^{14}/cm^2 is rather redundant in our device in that it makes excess oxide defects or traps to degrade the performance. The device with a dose of 1 × 10^{10}/cm^2 shows an effective suppression of degradation, which is better than that of the conventional hydrogen-annealed device.

The normalized gate current is plotted as a function of stress time for p-MOSFETs with 3-nm-thick gate oxides in Figure 6. The conventional, the hydrogen, and the deuterium processed devices were stressed at a constant V_g = 3.5 V voltage. The stress-induced leakage current

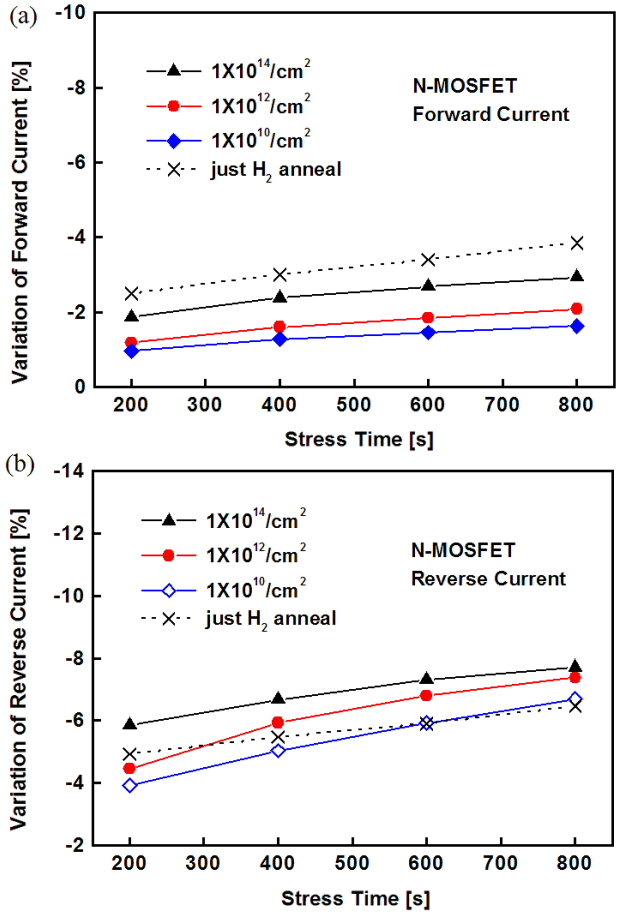

Fig. 5. Variations of the (a) forward, I_F, and the (b) reverse, I_R, saturation drain currents during HCI stress for deuterium-implanted n-MOSFETs. The implantation dose was changed from $1 \times 10^{14}/\mathrm{cm}^2$ to $1 \times 10^{10}/\mathrm{cm}^2$. The conventional device was annealed in a H_2 ambient at 450 °C.

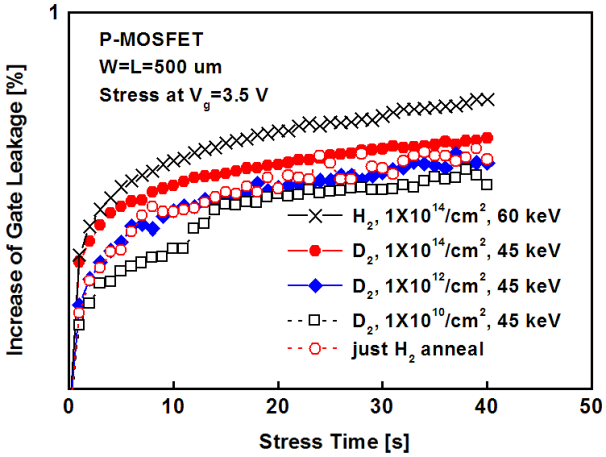

Fig. 6. Gate current transients during constant gate voltage, $V_g = 3.5$ V, for deuterium-implanted p-MOSFETs. These curves represent the evolution of defect generation.

is considered to be a monitor for defect generation in the

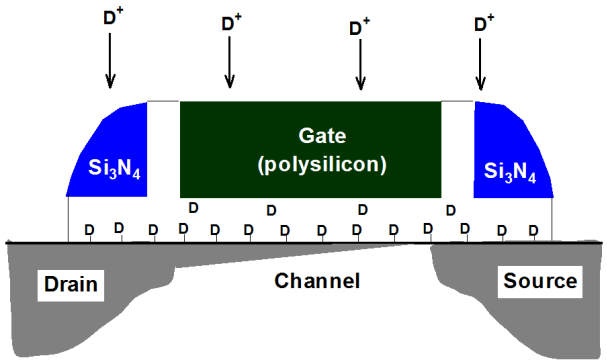

Fig. 7. Schematic diagrams of deuterium distribution in deuterium-implanted gate oxide. Deuterium atoms could exist uniformly at the Si/SiO_2 interface and in the bulk-SiO_2.

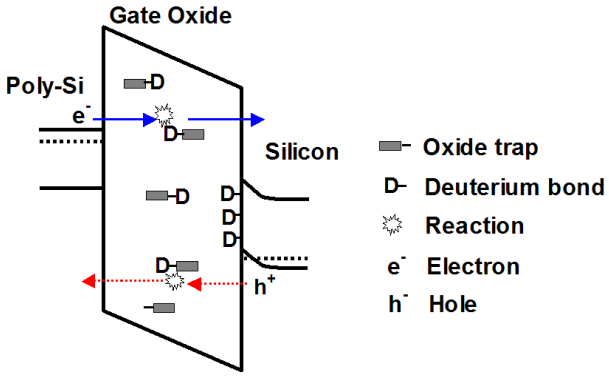

Fig. 8. Illustration for the deuterium bonds existing at the Si/SiO_2 interface and in the bulk-SiO_2, and the reaction with injected carriers.

gate oxide. From these curves, the deuterium process shows fewer defects than the hydrogen process, and the gate oxide implanted with deuterium, $1 \times 10^{12}/\mathrm{cm}^2$ dose, generates almost the same number of defects as the gate oxide annealed in H_2. The trap generation rate increases with the deuterium (or hydrogen) concentration in the gate oxide, which is the same result as in the hydrogen or the deuterium annealing process [10].

IV. DISCUSSION

In the annealing process, hydrogen or deuterium atoms reach the gate oxide layer through the upper layers, like aluminum, silicon oxide, silicon nitride, and polysilicon, by diffusion. In the case of deuterium annealing, low levels of deuterium are expected because the silicon nitride or polysilicon layer acts as a barrier to deuterium [8]. Therefore, the deuterium bond may not distribute uniformly along the channel area. The non-uniform distribution of deuterium bonds tends to preclude an isotope effect during electrical stress. By means of our suggested

implantation, the deuterium bonds could be distributed uniformly in the gate oxide layer, as shown in Figure 7.

Figure 8 illustrates the possible reaction for the generation of oxide traps in the deuterium- implanted n-MOSFETs gate oxide and an energy band diagram. When the deuterium bonds distribute through the gate oxide, two kinds of reactions, interface reactions and bulk reactions, may occur independently. The interface reaction involves deuterium release that could produce positive deuterium ions. The deuterium ions bonded with non-bridging atoms in the gate oxide bulk react with the energetic electrons or holes. The bond breakage is not accelerated as rapidly because deuterium is twice as heavy as hydrogen, and the dissociation by injected electrons or holes is suppressed. In the process of dissociation, the mass of the atom plays a significant role, and a large kinetic isotope effect is the consequence.

V. CONCLUSION

Using deuterium- and hydrogen-implanted gate oxides, we investigated the isotope effect for degradation of p- and n-MOSFET's performances under electrical stress. We found that Si-D bonds (instead of Si-H) play a major role in suppressing the generation of oxide traps. However, when the concentration of deuterium is redundant in the gate oxide, excess traps are generated and further degrade the performance. We found a suitable implant condition for our device under which the reliability is improved more than it is for the conventional hydrogen annealing process. Our result suggests a novel method to incorporate deuterium in the MOS structure for improved reliability.

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