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Matching behaviours of analogue NMOSFET parameters under hot-carrier stress

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Abstract
In this paper, we provide some experimental results of NMOSFET hot-carrier degradation for analogue circuit application. After hot-carrier stress, over the whole range of gate voltages, the drain current mismatch and output conductance are measured in the saturation region. Evidence of hole and electron trapping is found near the drain under low and high biased gate voltages, respectively, which is believed to be the cause of the variation of the output conductance during stress. Under low-gate-voltage stress, acceptor-like interface traps are also generated and compensate for the influence of trapped holes.

1. Introduction

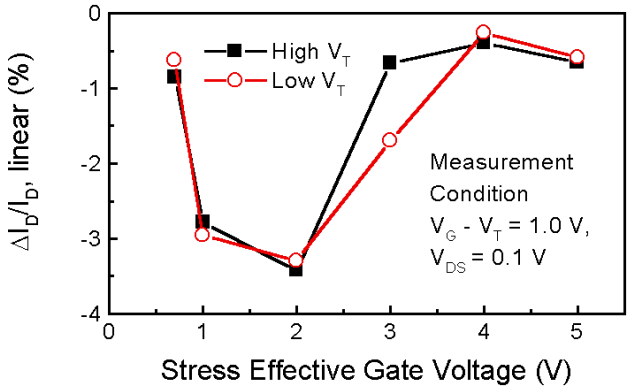
The operating points of MOS transistors in analogue and digital CMOS circuits differ significantly. Analogue devices usually operate in the saturation region with a quasi-static low gate voltage. Because analogue circuits usually use long-channel devices due to device-matching constraints, the influence of hot-carrier effects on analogue circuit performance has been believed to be minimal. However, for high-speed applications, submicrometre devices are necessary. As a result, the impact of hot-carrier degradation on the performance of analogue MOSFETs needs to be clearly understood [1, 2].

The typical characteristics of mismatch and output conductance, g_{ds}, for MOS devices are the real criteria for hot-carrier reliability in analogue CMOS applications [3–5]. Usually, drain current mismatch ($\Delta I_D/I_D$) is measured and modelled as a function of the affected device parameters. The degradation in the small-signal voltage gain is primarily due to the degradation in g_{ds} rather than in transconductance, g_m [2].

In this paper, we focus on the matching behaviour of the NMOSFET drain current and differential output conductance over the whole range of gate voltages in order to show the degradation mechanisms under different stress gate voltages. The analogue operation region could include the gate voltage range that results in maximum degradation. Moreover, we present a model, which is capable of explaining the degradation characteristics depending on stress gate voltage.

2. Experiment

The NMOS devices originate from a 0.35 μm CMOS process optimized for digital/analogue mixed applications, with a 7 nm gate oxide and with LDD profiles. The spacer length is approximately 180 nm, which leads to very smooth drain/source profiles and results in high values of differential output resistance, r_o. Devices with various values of L_{gate} (0.6, 0.7, 1.0 and 2.0 μm) but with the same gate width W_{gate} (3.0 μm) are employed to show the effect of the gate length. Devices from two different processes with low threshold-adjusted implants (B, 2.1 $\times$ 10^{13} cm^{-3} with 80 keV) and with high threshold-adjusted implants (B, 2.1 $\times$ 10^{13} cm^{-3} with 80 keV and BF^2, 1.5 $\times$ 10^{12} cm^{-3} with 80 keV) are used to perform the influence of channel dose, and their threshold voltages (V_T) are 0.4 and 0.7 V, respectively. The requirements of the analogue device are normally satisfied in standard CMOS technologies by reducing the channel doping level and, as a result, lowering V_T [6, 7]. For stresses, the effective gate voltages ($V_{G,eff} = V_G - V_T$) applied are from 0.7 to 5.0 V and the drain voltage (V_{DS}) is biased at 5.0 or 7.0 V. For characterization, the analogue bias condition is



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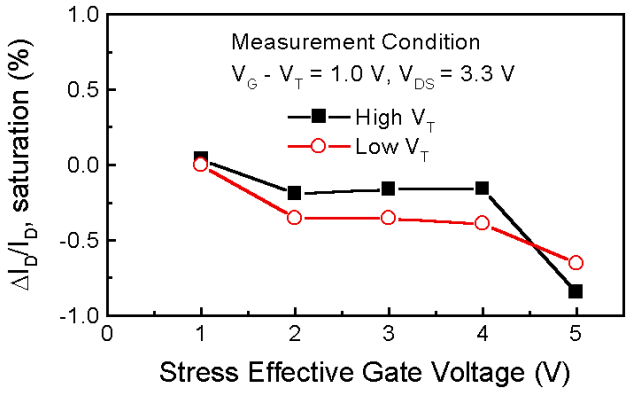


(*b*)

Figure 1. Drain current mismatch at the (*a*) linear and (*b*) saturation regions of NMOSFETs ($W_{gate}/L_{gate} = 3.0/2.0$) as a function of stress effective gate voltage. The threshold voltages for high V_T and low V_T devices are 0.7 and 0.4 V, respectively. Stress was achieved for 30 min at $V_{DS} = 5.0$ V.

used, that is $V_{G,eff} = 1.0$ V and $V_{DS} = 3.3$ V. For each data point shown in the figures, at least twenty devices on the same wafer are measured.

3. Results

The typical characteristics of NMOSFET current mismatch after hot-carrier stress are shown in figure 1 for different stress effective gate voltages. The linear-current mismatch in figure 1(*a*) can be divided into three distinct regions, each of which corresponds to a different degradation mechanism [2, 8]. For a low-gate-voltage stress condition ($V_{G,eff} \sim V_T$), the observed drain current is usually increased, which is assumed to be due to hole trapping [2]. However, our results do not show clear evidence of the increase in drain current. This implies that our stress condition ($V_{G,eff} = 0.7$ V, $V_{DS} = 5.0$ V) is insufficient to create prosperous hole trapping. For a mid-gate-voltage stress condition ($V_{G,eff} \approx 2$ V), the reduction of the drain current is completely due to the generation of acceptor-type interface states. The maximum interface state is generated around $V_{G,eff} = V_{DS}/2$, which corresponds to the maximum hot-carrier degradation. For a high-gate-voltage stress condition ($V_{G,eff} \geqslant 4$ V), electron trapping, which causes the observed decrease of the drain current, is believed to be dominant.

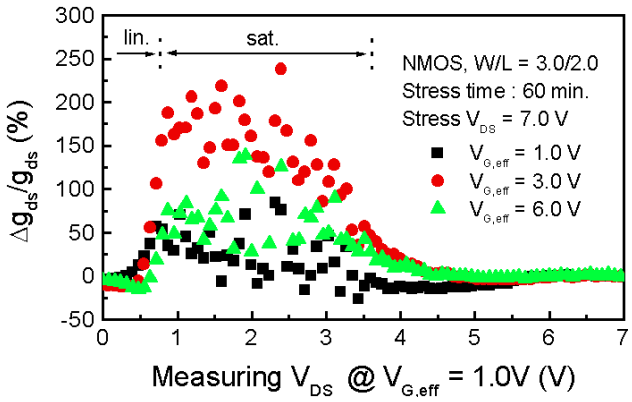


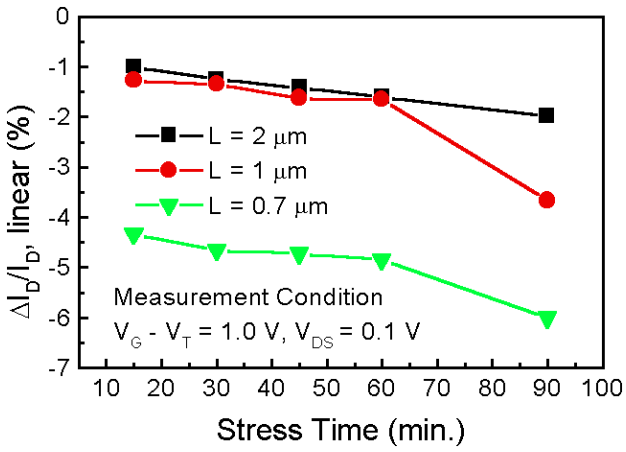
Figure 2. The variation of output conductance depending on stress effective gate voltage. The output conductance was measured at $V_{G,eff} = 1.0$ V and at the whole drain voltage. The stress time is typically 60 min.

When the device is biased in the saturation region, as for most analogue circuit applications, acceptor-type interface states generated during hot-carrier stress are mostly unoccupied (neutral) because of the lowered electron quasi-Fermi level near the drain. As a result, both hole and electron trapping will have large relative effects on device characteristics. This phenomenon will be dominant in higher-channel doped devices. Figure 1(*b*) shows that the current mismatch in the saturation region gradually changes from a positive value, due to hole trapping, to a negative value, due to electron trapping, as the stress gate voltage increases. Through the results of current mismatch in linear and saturation regions, we found that both hole trapping and acceptor-type interface states are generated during our low-gate-voltage stress condition, and then their influence appears alternately depending on the device measurement conditions. This phenomenon is also shown in figure 3.

Compared to high-channel-doped devices, low-channel-doped devices show decreased drain current at a mid-gate-voltage stress condition, which is because the electron quasi-Fermi level near the drain is shifted toward the conduction band. As a result more acceptor-type interface states are charged negatively. However, the difference between the results for two devices is quite small. Each data point presented here is the average value of test devices.

Figure 2 shows the variation of output conductance depending on the stress effective gate voltage measured over the whole range of drain voltages. The output conductance in the saturation region increases highly during the mid-gate-voltage stress condition ($V_{G,eff} = 3.0$ V), whereas it increases with a low rate for the low- and high-gate-voltage stress conditions, each of which corresponds to the voltage condition of hole and electron trapping. When a MOSFET enters the saturation region, the variation in g_{ds} is governed by channel-length modulation [9]. The expression for g_{ds} can be found, depending on the inversion-layer mobility μ and the length ΔL of the depletion in the channel region. We then obtain

$$\left.\frac{\Delta g_{ds}}{g_{ds}}\right|_{lin} = \frac{\Delta\mu}{\mu} - \frac{\Delta V_T}{(V_G - V_T - V_{DS})} \qquad (1)$$



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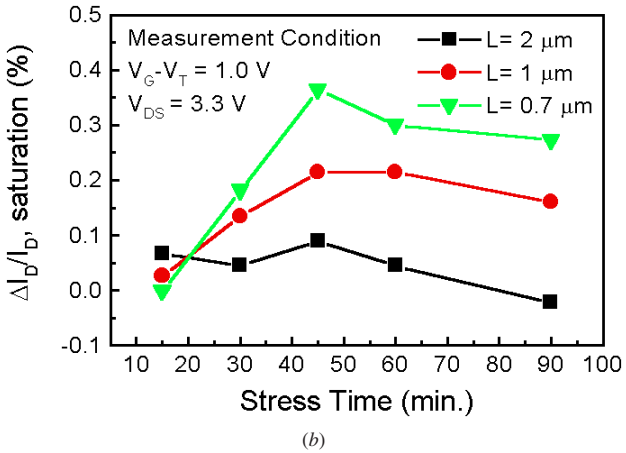

(*b*)

Figure 3. Drain current mismatch behaviours at the (*a*) linear and (*b*) saturation regions for the stressed NMOSFET under stress conditions: $V_G - V_T = 0.7$ V, $V_{DS} = 5.0$ V.

$$\left.\frac{\Delta g_{ds}}{g_{ds}}\right|_{sat} = \frac{I'_D}{I_D}\frac{d\Delta L'/dV_{DS}}{d\Delta L/dV_{DS}} - 1 \qquad (2)$$

where I'_D and $\Delta L'$ are the drain current and the depletion length of the channel region in the saturation region after hot-carrier degradation, respectively. When the device undergoes hot-carrier degradation at a low gate voltage, the threshold voltage, V_T, of the device is decreased, and hence the output conductance in the linear region is increased, as shown in figure 2.

The derivatives of ΔL with respect to V_{DS} at the saturation region are a key factor in the analysis of the output conduction degradation. We assume that, when the interface states generated during hot-carrier stress are unoccupied, the length of ΔL will be changed by a large amount responding to the variation of the biased V_{DS}; $d\Delta L'/dV_{DS} \gg \partial\Delta L/\partial V_{DS}$. However, the oxide trap charged with holes or electrons will directly increase or reduce the effective channel length and will tend to fix a channel length to a certain value during the variation of the biased V_{DS}. Hence, the length ΔL will respond with a slow rate to the variation of the biased V_{DS}; $d\Delta L'/dV_{DS} \geqslant d\Delta L/dV_{DS}$.

Figure 3 shows the matching behaviours of the linear and the saturation drain currents depending on channel length.

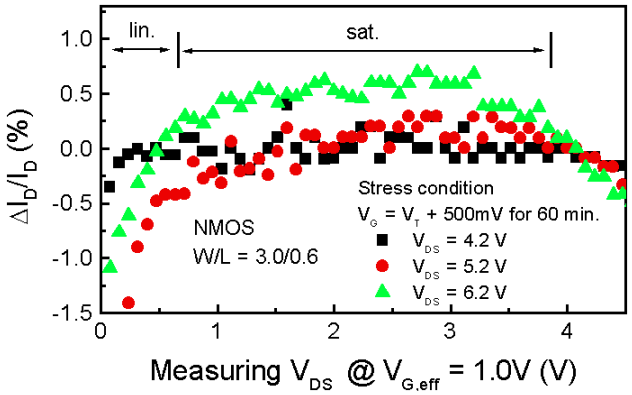

Figure 4. The variation of drain current depending on stress drain voltage. The drain current was measured at $V_{G,eff} = 1.0$ V and at the whole drain voltage. The stress time is typically 60 min.

The hot-carrier stress was achieved under the low-gate-voltage condition ($V_{G,eff} = 1.0$ V). The devices are manufactured by the low threshold-adjusted implantation process. During the first 60 min of stress, the drain current in the linear region is decreased, due to the influence of negatively charged acceptor-like interface states, while the drain current in the saturation region is increased, due to the influence of hole trapping. In figure 1, we also show the mismatch behaviour in our low-gate-voltage stress condition, resulting from the combination of hole and acceptor-like interface states. Here again, sometime after 60 min of stress, the linear drain current is decreased significantly, and the saturation drain current slowly decreases. This effect implies that acceptor-type interface states are generated dominantly for a long-time stress, even at the low-gate-voltage condition. The acceptor-type interface states can compensate for the influence of trapped positive charge, hole, in the current characteristics.

Our results rather disagree with those of Stadlober [8]. This discrepancy probably comes from the difference of device structure; we used an LDD profile and shorter channel compared to Stadlober's devices. In our LDD device, hot-holes will be trapped in the gate oxide near the drain rather than in the spacer oxide above the LDD because of the lower gate voltage compared to the drain voltage during stress. However, the interface traps can be created above the LDD region, and hence degrade the drain series resistance during stress. Our long-channel device ($L = 2.0$ μm) shows no clear sign of an increase in saturation drain current during stress. This means that the decrease of ΔL due to the trapped hole near the drain is negligible for the total channel length.

Figure 4 shows the variation of the drain current measured at the whole drain voltage. The stress effective gate voltage is fixed to 0.5 V, and the stress drain voltage is changed from 4.2 V to 6.2 V. As the stress drain voltage is increased, the amount of hole trapping is also increased. Also, under the same stress condition, the drain current is slowly increased up to the end of the saturation region. This means that hole trapping is generated in the gate oxide above the length of ΔL during stress, and its effect appears gradually as the drain voltage increases during measurement. At the end of the saturation region, the length of ΔL will reach a maximum, and

then the almost trapped hole will contribute to the increase of the saturation drain current.

4. Conclusions

The characteristics of current mismatch after hot-carrier stress show that oxide charges (both hole and electron) are trapped near the drain for low- and high-gate-voltage stress conditions. The oxide traps are believed to fix the effective channel length so that the variation rates of channel length to biased drain voltage become small, which correspond to the small variation of output conductance in the saturation region after hot-carrier stress. Unoccupied acceptor-type interface states are generated for a mid-gate-voltage stress condition and result in a large increased output conductance after hot-carrier stress. At the start of hot-carrier stress under low gate voltage, holes are trapped in the gate oxide near the drain, and hence increase the saturation drain current. However, in long-term stress, acceptor-like interface traps are generated dominantly and compensate for the influence of trapped-hole charges.

Acknowledgment

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